Conduction regime in innovative carbon nanotube via interconnect architectures

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We report on the electrical properties of multiwall carbon nanotube based via interconnects over a broad range of temperature and bias voltage. By using innovating processing techniques, high density nanotube vias have been fabricated from single damascene and double damascene via architectures with diameters down to 140 nm. For single damascene structures, resistances as low as 20 Ω have been achieved for 300 nm via size. Further measurements show that the conductance increases with temperature following an exponential law, which can be interpreted in terms of a disordered quasi-one dimensional conduction regime. © *2007 American Institute of Physics*.
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The main route toward the goal of achieving faster computer chips is in scaling down the size of transistors and interconnections, thereby allowing a higher density of components. Although this route has been pursued without interruption since the early days of microelectronics, further progress may be hindered by short circuits, cross-talk, and temperature overheating phenomena when reaching the nanoscale. In particular, severe issues such as electromigration or not sufficient current density capabilities inferior to 10^7 A/cm^2 could jeopardize the use of copper as conducting material for next generation interconnects.[1] A crossover between copper and advanced technologies is anticipated for 22 nm nodes. Carbon nanotubes (CNTs) are promising materials for micronanoelectronics interconnections due to their outstanding properties[2] and are currently the subject of intense studies.[3–5] Although current densities of up to 10^9 A/cm^2 have already been achieved, the CNT vias resistances are still one order of magnitude higher than those of copper,[4] and further work is needed to make them competitive alternatives. Additionally, intensive electrical characterizations of fabricated devices, such as $I(V)$ variability, are crucial for optimizing realistic circuit simulation.[6–8] This work is focused on investigating the conduction mechanisms in densely packed multiwalled carbon nanotubes (MWCNTs) via interconnections down to 140 nm in diameter on 200 mm silicon wafers.

Two innovative processes have been developed to achieve both single damascene (SD) and dual damascene (DD) via architectures. Promisingly, the double damascene approach has been implemented and the resulting CNT vias conduction properties were analyzed. This structure is very interesting since the top level patterns are already aligned and achieved before filing up the vias hole with CNTs. No further lithography and etching steps are then needed. Inside each via hole, a density of 5×10^{10} MWCNTs/cm^2 has been obtained. Interestingly, at large bias, the conductance increases until reaching low resistances down to 20 Ω which have been obtained for 300 nm wide vias at high-bias voltage.

Transport measurements in wide range of temperature and bias voltage have been performed on about ten samples and consistent results were obtained. The main result is a strong temperature dependence of the low-bias conductance, with an increase of about three orders of magnitude for a temperature change from 50 to 300 K. This temperature behavior is analyzed in terms of a disordered one-dimensional conduction regime.[9,10] Micro-Raman spectroscopy measurements[11] performed directly on the vias have confirmed the presence of an important density of defects and disorder, presumably due to low temperature growth (520 °C). In the following, the fabrication of such interconnects together with the experimental measurement setup is firstly detailed, followed by the current-voltage analysis.

The single damascene via architecture is obtained as follows: a lower metal level constituted by copper lines and α-SiOCH is made. Then, a 300 nm SiO_2 is deposited using plasma enhanced chemical vapor deposition (CVD) method with tetraethoxysilane. After opening vias holes from 140 to 300 nm in width, a 10 nm layer has been deposited by evaporation of Al. The conductivity of Al is at least 20 times higher than the conductivity of Ta/TiN layers used by other groups.[3,4] This could allow us to decrease the overall via resistance. A 3 nm Ni catalyst layer is then deposited by e-beam evaporation. The distance between the substrate and the Ni source is around 1 m, leading to a very directional catalyst deposition at the bottom of via holes. Parasitic Al and Ni layers on the top surface are further removed by chemical mechanical polishing (CMP). In order to prevent catalyst poisoning at the bottom of vias during CMP, a protective resin layer is previously deposited and further etched by O_2/CF_4 plasma stripping. The dual damascene via structure is performed on a metal level made of copper lines sur-

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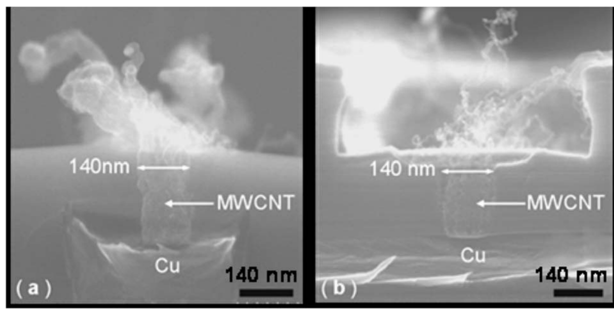

FIG. 1. (a) 140 nm wide single damascene via structure, filled up with MWCNTs with average size of 15 nm growing from the lower copper electrodes. (b) 140 nm wide double damascene structure with average tube diameteral about 8 nm.

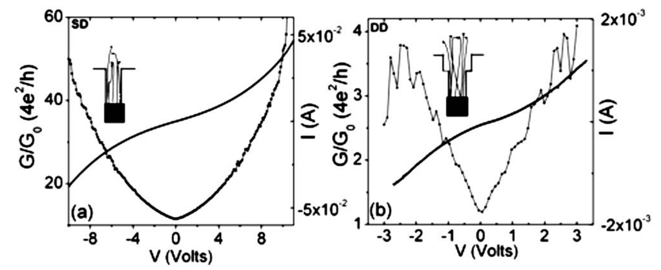

FIG. 2. Two probe measurement at 293 K for (a) a single 300 nm diameter SD via and (b) a single 200 nm diameter DD via. Continuous $I(V)$ curves are given by the right y scale. The corresponding conductances are given by the black dotted broken line with the left y scale. Schematic representations of SD and DD architectures are shown in the insets.

rounded by α-SiOCH. A 600 nm α-SiOCH layer is deposited over a 40 nm SiCN etching stop layer. Via holes and upper level trenches (aligned on vias) are patterned prior to the CNT filling. The same Al/Ni stack is then deposited. Since parasite Ni has to be deactivated in the upper metal trenches, a 20 nm Al is deposited with an angle of 45° with respect to via axis. Since the silicon wafer substrate is turning along the axis of via holes, only the Ni deposited at the bottom of the vias remains uncovered and thus active. A more detailed explanation for achieving SD and DD architectures can be found in Ref. 12. CVD growth method is then performed at 520 °C with a C_2H_2/H_2 mixture at 2 mbars and only MWCNT-like structures are obtained. SD and DD structures with diameters from 140 to 300 nm and filled up with nanotubes have been achieved. Figure 1 represents scanning electron microscopy images taken with a Hitachi P5000 at 30 kV of the two different architectures. For SD structure, the nanotube density is about 5×10^{10} nt/cm^2 with an average diameter of 15 nm. DD MWCNTs show smaller average diameter size of 8 nm possibly due to lower gas flow at the bottom.

A 300 nm thick AuPd alloy is sputtered and patterned to perform top contacts. This metal is believed to match with the work function of the nanotubes.[13] Since sputtering alloy is not collimated, the CNTs are surrounded by metal over 100 nm along their axis above the via hole. This provides Ohmic contacts with low resistance. Since our CNTs are twisted around each other and densely packed, no free space should be available for the metal to form a path from top to bottom contacts. Additionally, given that in our setup MWCNTs exhibit tip growth, the bottom contacts are self-performed during growth on the copper layer. Some inner shells could therefore be connected at this point. Two probe measurements were performed in the voltage range from −10 to +10 V at temperatures between 50 and 300 K. To evaluate the resistance of the whole measurement setup, the AuPd sheet resistance is measured with the two probe system and an Ohmic behavior of 80 Ω is found over the full −10, +10 V range. This resistance is considered as a measurement setup contact resistance and has to be subtracted from the experimental values. Although via holes down to 140 nm in diameter have been achieved, 300 nm wide SD and 200 nm wide DD have been electrically tested. Further experiments on 140 nm wide vias are in progress.

We did not notice any hysteresis after repetitive $I(V)$ high-bias measurements which ensures that contact formation does not occur during voltage sweeping. Since the DD vias measured were 200 nm in diameter, only a few tens of nanotubes participate in the conduction. One can thus expect to observe individual CNT fingerprints. Figure 2(b) shows the current as well as the conductance as a function of the bias voltage for a DD structure of 200 nm in diameter. A non-Ohmic behavior is observed. The conductance $G=(dI/dV)$ increases linearly with the bias voltage, reaching an equivalent resistance of 2.5 kΩ before dropping at about ±2.6 V. Similar behavior in transport through a single MWCNT has been reported by Liang *et al.*[14] They explained it by noticing that the number of available channels $M(E)$ as a function of energy, which determines the upper limit for the conductance, follows essentially the same trend as the observed conductance-voltage characteristics. Actually, $M(E)$ increases linearly for low bias until it reaches a certain diameter dependent bias threshold when it starts to decrease. The resistance of few kilohms is quite high and most presumably due to the imperfect structure of low temperature grown nanotubes. Figure 2(a) illustrates electrical tests on a 300 nm SD diameter via interconnect. These measurements have been performed several times on different single via holes and reproducible trends with low-bias resistances between 100 Ω and 1 kΩ have been found. We attribute the higher resistances observed for DD to smaller diameter of DD via hole (200 vs 300 nm) and also to the smaller radii of the tubes grown in the DD (8 vs 15 nm) which result in a reduced number of available conduction channels. Another noticeable feature is that the conductance rises in a nonlinear way contrary to DD structures at high voltages, probably due to Zener tunneling from contacts through energy activated nanotube subbands.[15] At high 10 V bias, the resistance drops to 20 Ω while the current flowing reaches 50 mA, which corresponds to a value of 7×10^7 A/cm^2 per via. Assuming around 20 nanotubes for a 300 nm interconnect, the current density is estimated to be about 2.10^8 A/cm^2 per nanotube.

Further investigations have been performed at low temperatures. A strong temperature dependence of the low-bias conductance, with an increase of about three orders of magnitude for a temperature change from 50 to 300 K has been observed. On the left of the inset of Fig. 3, the conductance versus voltage for a SD via of 300 nm in diameter is shown; different curves correspond to different temperatures. We interpret our experimental results in terms of a quasi-one-dimensional disordered conductor.[9] The theory for these systems[9,10] predicts a low-bias conductance $G_{0\ \mathrm{V}}$ which varies exponentially with temperature T as $G_{0\ \mathrm{V}} \propto \exp - C/\sqrt{T}$, where C is a parameter whose value increases with the defects density in the material. The picture is that of a system

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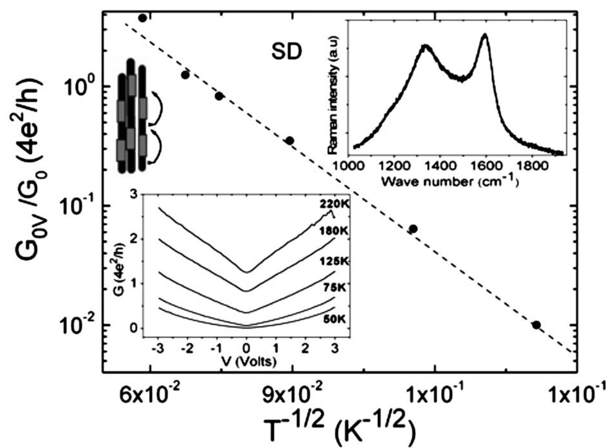

FIG. 3. Main frame: black dots represent low-bias conductances vs temperature $T^{-0.5}$ in a log-normal scale. The linear fitting theory is drawn as a dashed line. The single fitting parameter is $C=34\pm1$ $K^{0.5}$. Right inset: micro-Raman spectra of SD vias. A large D band around 1355 cm^{-1} is observed confirming the presence of disorder. Left insets: conductance curves vs voltage for different temperatures on a SD 300 nm diameter via hole. A scheme of hopping processes (arrows) through defects along the tubes is also shown.

which is divided into fragments owing to the presence of defects. Carriers tunnel between these fragments through temperature-dependent hopping processes (see the left scheme on Fig. 3). In Fig. 3, the low-bias conductances have been plotted as a function of $T^{-0.5}$ in a log scale. The theory nicely fits our data with a single fitting parameter $C=34\pm1$ $K^{0.5}$. Previous experiments[10] have also reported a good agreement with this theory, although the estimated C values were one order of magnitude smaller than those reported here. This difference can be attributed to the fact that the data in Ref. 10 were obtained by using purified arc discharge nanotubes, thus, improving the tube quality and reducing the density of defects. In our case, a higher density of defects, and thus a higher C value, is expected since nanotubes are grown at lower temperatures. Further micro-Raman experiments on SD vias confirm the presence of a large D band (see left inset of Fig. 3) which is associated to the presence of disorder and defects.[11] We have also tried to fit our data using Lutinger liquid (LL) theory[16] but no good agreement could be found. In this theory, power law trends of $G_{0\text{ V}}\sim T^{\beta}$ (at fixed voltage) and $G\sim V^{\beta}$ (at fixed temperature) are predicted, as well as a universal collapsing of $(G_{0\text{ V}}/G_0)/T^{\beta}$ versus eV/k_BT independently of the sample. In contrast, as seen on Fig. 4, our data show that at fixed low bias $G_{0\text{ V}}\sim T^{\beta}$ with $\beta=3.2>1$ and $G\sim V^{\alpha}$, α being a strong temperature dependent exponent ranging from 1 above 180 K to 2.6 at 50 K. Moreover, after rescaling all conductances curves, the universal behavior predicted by LL theory (i.e., collapse of the curves) is not satisfied (see inset of Fig. 4). Thus, the transport regime in our interconnects cannot be described within the LL theory.

In summary, both single and double damascene carbon nanotube interconnects down to 140 nm in diameter have been fabricated using low temperature CVD growth. The electrical behaviors of both structures have been investigated

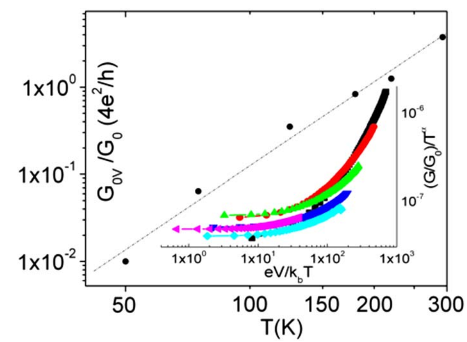

FIG. 4. (Color online) Power law dependence fitting of the low bias conductance with temperature: $G_{0V}\sim T^{3.2}$. Inset: rescaled conductance curves using Lutinger liquid theory.

over wide temperature and voltage ranges. For the single damascene structures, high-bias resistances down to 20 Ω have been reached. The temperature behavior suggests a disordered quasi-one-dimensional conduction regime confirmed by Raman spectroscopy showing a high density of defects. The route followed in this study offers advantages in the way toward building large scale CNT interconnections for industrial applications. This study could also foster further theoretical simulations.

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